AWM1271

EXPANDABLE FOUR-LINE DECODER - DRIVER

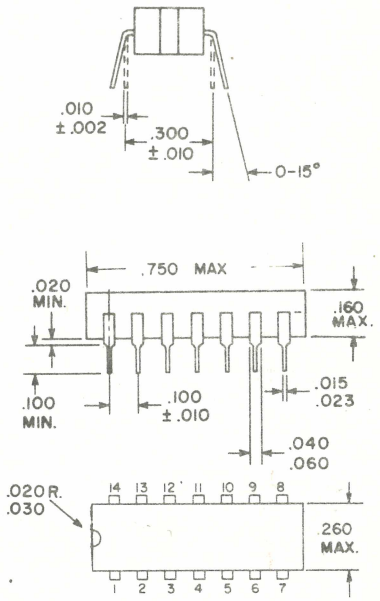
DESCRIPTION

The AWM 1271 is a DTL MSI module providing a one-out-of-four decoding function of a 3 bit binary code. A select pin is provided so that, for the select pin low, the binary codes 0 to 3 are decoded, with no action on 4 to 7; while 4 to 7 are decoded, with no action on 0 to 3, with this pin high. Thus, two packages together provide an 8 line decoder function. Each of the four outputs have a 50mA sinking capability and are "open collector". Three separate inhibit inputs are provided.

GENERAL CHARACTERISTICS

Package:	14 pin DIL ceramic
Max. storage temp:	140°C
Operating temp. range:	0°C to 70°C
Supply voltage:	4.5 to 5.5V
Max. input to any pin:	+ 5.5V
Min. input to any pin:	- 0.5V
Logic levels:	compatible with TTL/DTL
Load sinking capability:	50mA per line
Address set-up time:	50ns (typ)
Inhibit propagation time:	30ns (typ)
Power dissipation:	125mW

DIMENSIONAL OUTLINE



(Dimensions in Inches)

PIN CONNECTIONS

1. Inhibit A
2. Select
3. Address a_3
4. Address a_2
5. Address a_1
6. Inhibit B
7. Inhibit C
8. Ground
9. Line 1 or 5
10. Line 2 or 6
11. Line 3 or 7
12. Line 4 or 8
13. Ground
14. Pos. Supply

Pins (8, 13) are internally connected

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AWA

INTEGRATED CIRCUIT

AWV PRIVATE MAIL BAG ERMINGTON 2115 TELEGRAMS "VALVES" ERMINGTON TELEPHONE 638 0411

TRUTH TABLE

(LOGIC "1" = HIGH) ALL INHIBITS HIGH.

a_1	a_2	a_3	SELECT = 0				SELECT = 1			
			1	2	3	4	1	2	3	4
0	0	0	0	1	1	1	1	1	1	1
1	0	0	1	0	1	1	1	1	1	1
0	1	0	1	1	0	1	1	1	1	1
1	1	0	1	1	1	0	1	1	1	1
0	0	1	1	1	1	1	0	1	1	1
1	0	1	1	1	1	1	1	0	1	1
0	1	1	1	1	1	1	1	1	0	1
1	1	1	1	1	1	1	1	1	1	0

NOTE :- ALL OUTPUTS HIGH IF I_A or I_B or I_C IS LOW.

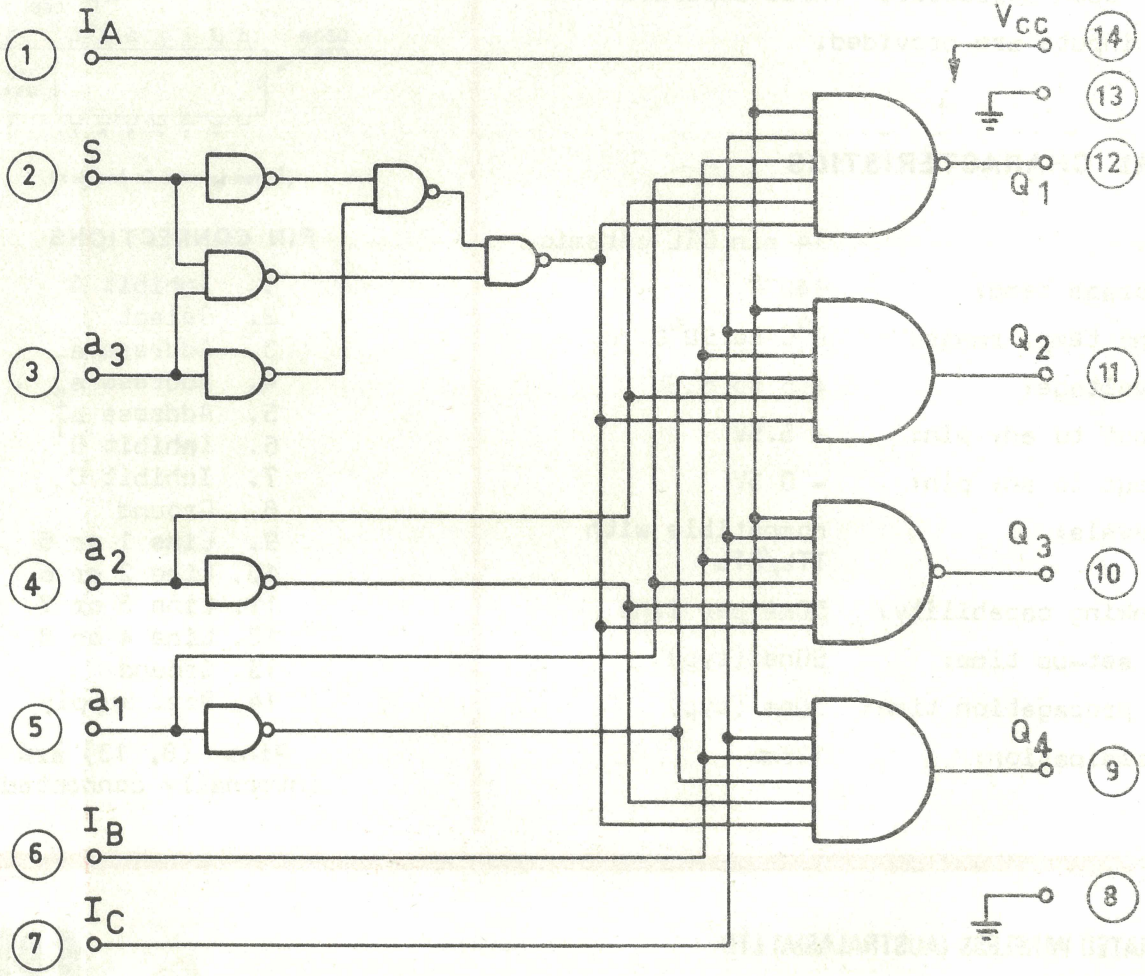

FIG. 1. FUNCTIONAL SCHEMATIC.

PIN	FUNCTION	PARAMETER ($T = 25^{o}C$)	FORCING FUNCTION	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS
1	Inhibit[1] A	High state:					
		voltage V_{IH}		2		5.5	V
		current I_{IH}	V_{IH} = 5V	0		.01	mA
		Low state:					
		voltage V_{IL}		-0.5		1.0	V
		current I_{IL}	V_{IL} = 0V	-1.5	-2	-2.5	mA
2	Address select	High state:					
		voltage V_{IH}		2		5.5	V
		current I_{IH}	V_{IH} = 5V	0		0.01	mA
		Low state:					
		voltage V_{IL}		-0.5		1.2	V
		current I_{IL}	V_{IL} = 0V	-1.5	-1.8	-2.0	mA
3	Address line a_3	See (2)					
4	Address line a_2	See (1)					
5	Address line a_1	See (1)					
6	Inhibit[1] B	See (1)					
7	Inhibit C	See (1)					
8	Ground[2] (Common with 13)						
9	Output line[3] 1 or 5 (Q_1)	High state:					
		current I_{OH}	V_{OH} = 5V	0		0.05	mA
		Low state:					
		voltage V_{OL}	I_L = 50mA	0.3	0.38	0.43	V
		current I_{OL}				50	mA
10	Output line 2 or 6 (Q_2)	See (9)					
11	Output line 3 or 7 (Q_3)	See (9)					
12	Output line 4 or 8 (Q_4)	See (9)					
13	Ground[2] (Common with 8)						
14	Positive supply	Voltage		4.5	5	5.5	V
		Current	V_{CC} = 5V, all inputs high	18	20	25	mA

Notes
1. Outputs disabled (high) for inhibit low.
2. It is recommended that common pins be externally shorted.
3. Open collector output.

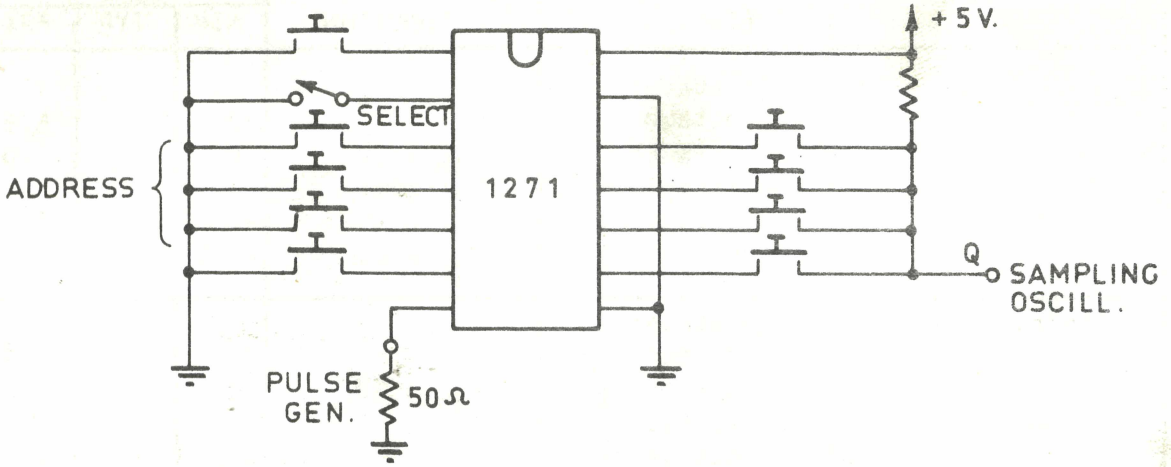

FIG. 2. FUNCTION AND SPEED TEST.

TYPICAL SWITCHING PARAMETERS		
PROP. DELAY: INHIBIT TO OUTPUT	t_{p+}	25 ns
	t_{p-}	30 ns
ADDRESS SET UP TIME	t_a	50 ns

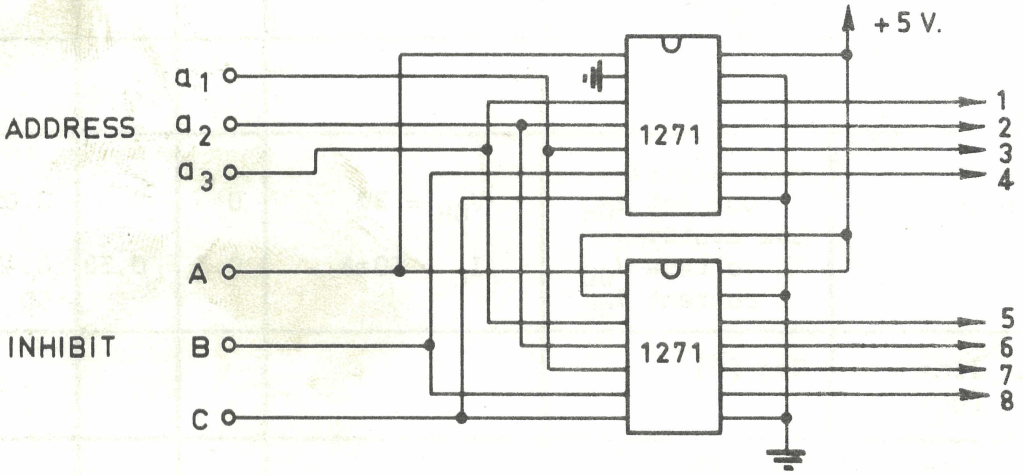

FIG. 3. INTERCONNECTION AS 8-LINE DECODER.

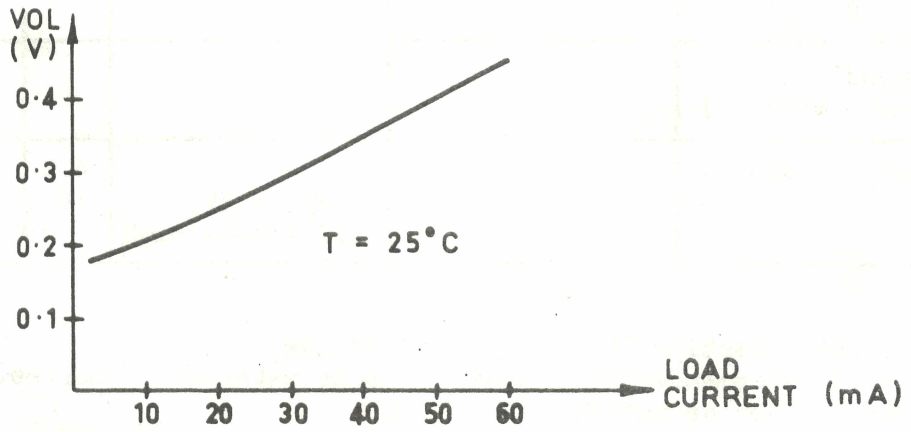

FIG. 4. TYPICAL OUTPUT LOADING CURVE (PER LINE.)